

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	281	(712/237).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2006/04/17 12:01
L2	186	(712/238).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2006/04/17 12:01
L3	443	(712/239).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2006/04/17 12:02
L4	198	(712/235).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2006/04/17 13:33
L5	0	((speculat\$4 and architect\$5) near4 (branch adj1 target)) near4 ((allocat\$3 or assign\$3 or mak\$3) near4 buffer\$1 near4 entr\$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/17 13:35
L6	0	((speculat\$4 and architect\$5) near4 (branch adj1 target)) with ((allocat\$3 or assign\$3 or mak\$3) near4 buffer\$1 near4 entr\$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/17 13:35
L7	0	((speculat\$4 and architect\$5) near4 (branch adj1 target)) same ((allocat\$3 or assign\$3 or mak\$3) near4 buffer\$1 near4 entr\$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/17 13:35
L8	0	((speculat\$4 and architect\$5) with (branch adj1 target)) same ((allocat\$3 or assign\$3 or mak\$3) with (buffer\$1 near4 entr\$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/17 13:35
L9	0	((speculat\$4 and architect\$5) with (branch adj1 target)) same ((allocat\$3 or assign\$3 or mak\$3) with (buffer\$1 near4 entr\$3)).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/17 13:35
L10	0	((speculat\$4 and architect\$5) with (branch near4 target)) same ((allocat\$3 or assign\$3 or mak\$3) with (buffer\$1 near4 entr\$3)).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/17 13:35

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L11	0	((speculat\$4 and architect\$5) with (branch near4 target)) same ((allocat\$3 or assign\$3 or mak\$3) with (buffer\$1 with entr\$3))).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/17 13:35
L12	0	((speculat\$4 and architect\$5) same (branch with target)) same ((allocat\$3 or assign\$3 or mak\$3) same (buffer\$1 with entr\$3))).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/17 13:36
L13	0	((speculat\$4 and architect\$5) same (branch with target)) same ((allocat\$3 or assign\$3 or mak\$3) same (buffer\$1 same entr\$3))).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/17 13:56
L14	0	((speculat\$4) with (branch with target)) same ((allocat\$3 or assign\$3 or mak\$3) with (buffer\$1 with entr\$3))).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/17 13:56
L15	1	((speculat\$4) with (branch with target)) same ((allocat\$3 or assign\$3 or mak\$3) with (buffer\$1 with entr\$3)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/17 13:57
S1	40	speculat\$4 near4 (branch adj1 target)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/08 13:36
S2	3	(branch adj1 target adj1 buffers) near4 speculativ\$4	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2003/06/12 10:28
S3	3	(branch adj1 target adj1 buffers) with speculativ\$4	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2003/12/10 11:35
S4	55	branch adj1 target adj1 buffers	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2003/06/12 11:32
S5	82	((712/239).CCLS.) and (branch adj1 target adj1 buffer\$1)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2003/06/12 14:53
S6	8	(("5515518") or ("6321328") or ("5842008") or ("5553255") or ("6185668") or ("5732253") or ("6067616") or ("6553488")).PN.	USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2003/06/16 07:52
S7	210	(712/237).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2003/12/10 10:59
S8	153	(712/238).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2003/12/10 10:59

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S9	326	(712/239).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2003/12/10 10:59
S10	134	(712/235).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2003/12/10 11:00
S11	12	(branch near2 buffers) same speculativ\$4	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2003/12/10 11:00
S12	8	(US-5842008-\$ or US-5515518-\$ or US-6553488-\$ or US-6067616-\$ or US-5732253-\$ or US-6321328-\$ or US-6185668-\$ or US-5553255-\$). did.	USPAT	OR	OFF	2003/12/10 11:33
S14	22	branch\$3 near4 (speculative near4 (target adj1 buffer))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/07/09 12:02
S15	22	(speculative near4 (branch\$3 adj1 target adj1 buffer))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/07/09 12:03
S16	49	(speculative with (branch\$3 adj1 target adj1 buffer))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/07/09 14:49
S17	49	(speculative with (target adj1 buffer))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/07/09 14:49
S18	103	(speculative with (branch\$3 near4 buffer))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/07/09 14:49
S19	217	(712/237).CCLS.	USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/07/09 14:50
S20	140	(712/238).CCLS.	USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/07/09 14:50

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S21	314	(712/239).CCLS.	USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/07/09 14:50
S22	110	(712/235).CCLS.	USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/07/09 14:50
S23	1	("6513109").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/07/09 15:19
S24	247	(712/237).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/12/06 17:10
S25	164	(712/238).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/12/06 17:10
S26	380	(712/239).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/12/06 17:10
S27	166	(712/235).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/12/06 17:10
S28	1	("5481693").PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/07 14:10
S29	1	("5685009").PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/07 14:11
S30	28	(float\$3 adj1 point adj1 units) near4 multiple	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/08 13:37
S31	255	(712/237).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/05/12 16:43

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S32	167	(712/238).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/05/12 16:43
S33	399	(712/239).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/05/12 16:43
S34	173	(712/235).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/05/12 16:43
S35	107	(speculative with (branch\$3 near4 buffer))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/12 17:11
S36	52	(speculative with (branch\$3 adj1 target adj1 buffer))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/12 17:11
S37	4	(branch adj1 target adj1 buffers) same speculativ\$4	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/12 17:13
S38	4	(branch adj1 target adj1 buffers) same speculativ\$4	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/12 17:13
S39	270	(712/237).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/10/28 10:34
S40	179	(712/238).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/10/28 10:34
S41	422	(712/239).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/10/28 10:34
S42	182	(712/235).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/10/28 10:34



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- #1 (((speculative <or> speculate <or> speculating <or> speculated)
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buffers))))<in>metadata)
- #2 (((speculative <or> speculate <or> speculating <or> speculated)
<sentence> (branch <near/2> target <near/2> (buffer <or>
buffers))))<in>metadata)
- #3 (((speculative <or> speculate <or> speculating <or> speculated)
<sentence> (branch <sentence> target <sentence> (buffer <or>
buffers))))<in>metadata)
- #4 (((speculative <or> speculate <or> speculating <or> speculated)
<paragraph> (branch <sentence> target <sentence> (buffer
<or> buffers))))<in>metadata)
- #5 (((speculative <or> speculate <or> speculating <or> speculated
<or> prediction <or> predicted <or> predicting) <sentence>
(branch <sentence> target <sentence> (buffer <or> buffers))))
<in>metadata)

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speculative + architectural + branch + target

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The Effects of Mispredicted-Path Execution on **Branch** Prediction Structures - group of 5 »

S Jourdan, TH Hsing, J Stark, YN Patt - Proceedings of the International Conference on Parallel ..., 1996 - doi.ieeecomputersociety.org

... ing to the checkpoint holding the mispredicted **branch**, the subsequent **speculative** predictions can ... technique can still be used if the **architectural** state is ...

Cited by 26 - [Web Search](#)

DAISY: Dynamic Compilation for 100% **Architectural** Compatibility - group of 19 »

K Ebcioğlu, ER Altman - ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE, 1997 - ieeexplore.ieee.org

... and why is it different than an ONPAGE **branch**? ... 2.1 Essential **Architectural** Features for Ag- gressive Reordering ... the usual support for **speculative** execution and ...

Cited by 177 - [Web Search](#) - [BL Direct](#)

A Comprehensive Instruction Fetch Mechanism for a Processor Supporting **Speculative** Execution - group of 6 »

TY Yeh, YN Patt - MICRO-ANNUAL WORKSHOP THEN ANNUAL INTERNATIONAL SYMPOSIUM-, 1992 - ieeexplore.ieee.org

... If the **branch** is an indirect **branch**, its **target** address is not available until the source re- gister value is calculated. **Speculative** updates of **branch** history ...

Cited by 67 - [Web Search](#) - [BL Direct](#)

Execution-based prediction using **speculative** slices - group of 18 »

C Zilles, G Sohi - ACM SIGARCH Computer Architecture News, 2001 - doi.ieeecomputersociety.org

... is assumed for providing **target** addresses, which ... state (through prefetching and **branch** prediction hints ... This **speculative** nature provides significant flexibility ...

Cited by 105 - [Web Search](#) - [BL Direct](#)

Supporting Highly-**Speculative** Execution via Adaptive **Branch** Trees - group of 8 »

TF Chen - HPCA, 1998 - ieeexplore.ieee.org

... alternative is used as a **branch** path predictor for **speculative** execution. ... The two **branch** addresses on its fall-through path (B001) and **target** path (B011 ...

Cited by 8 - [Web Search](#)

Target Prediction for Indirect Jumps - group of 9 »

PY Chang, E Hao, YN Patt - ACM SIGARCH Computer Architecture News, 1997 - portal.acm.org

... cache was designed for highly **speculative** machines, where ... be several targets for each indirect **branch** and each ... history, a large number of **target** cache **entries** ...

Cited by 58 - [Web Search](#) - [BL Direct](#)

Dynamic **Branch** Prediction for a VLIW Processor - group of 7 »

J Hoogerbrugge - IEEE PACT, 2000 - doi.ieeecomputersociety.org

... for a superscalar, where dynamic **speculative** exe- cution ... 5. Selective Dynamic **Branch** Prediction VLIW processors typically expose micro-**architectural** details in ...

Cited by 15 - [Web Search](#)

Dynamic Strands: Collapsing **Speculative** Dependence Chains for Reducing Pipeline Communication - group of 7 »

P Sassone, DS Wills - Proceedings of the International Symposium on ..., 2004 - portal.acm.org

... the IPC gains from the **speculative** and double ... Table 2. **Architectural** parameters used for all ... gshare **Branch** History Table 4096 **entries** **Branch** **Target** Buffer 2048 ...

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Two-level adaptive training **branch** prediction - group of 12 »



speculative + architectural + branch + target + buffers Search

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Scholar Results 1 - 10 of about 999 for **speculative + architectural + branch + target + buffers**. (2.18 seconds)

Reducing the cost of branches - group of 2 »

S McFarling, J Hennessy - 13th Annual International Symposium of Computer Architecture, 1986 - portal.acm.org
... Proceedings of the first international symposium on **Architectural** support for ... JKL
and Smith, AJ., "**Branch** Prediction Strategies and **Branch Target** Buffer Design ...
[Cited by 168](#) - [Web Search](#)

The Effects of Mispredicted-Path Execution on **Branch** Prediction Structures - group of 5 »

S Jourdan, TH Hsing, J Stark, YN Patt - Proceedings of the International Conference on Parallel ..., 1996 - doi.ieeecomputersociety.org
... ing to the checkpoint holding the mispredicted **branch**, the subsequent **speculative**
predictions can ... history buffer used to restore the **architectural** state of ...
[Cited by 26](#) - [Web Search](#)

A Comprehensive Instruction Fetch Mechanism for a Processor Supporting **Speculative** Execution - group of 6 »

TY Yeh, YN Patt - MICRO-ANNUAL WORKSHOP THEN ANNUAL INTERNATIONAL SYMPOSIUM-, 1992 - ieexplore.ieee.org
... If the **branch** is an indirect **branch**, its **target** address is not available until the
source register value is calculated. **Speculative** updates of **branch** history ...
[Cited by 67](#) - [Web Search](#) - [BL Direct](#)

Fast and Accurate Instruction Fetch and **Branch** Prediction - group of 12 »

B Calder, D Grunwald - ACM SIGARCH Computer Architecture News, 1994 - portal.acm.org
... address space means **branch target buffers** become more expensive ... During a related
study on the **architectural** features used by object-oriented languages, such ...
[Cited by 78](#) - [Web Search](#) - [BL Direct](#)

Instruction Cache Fetch Policies for **Speculative** Execution - group of 16 »

D Lee, JL Baer, B Calder, D Grunwald - ACM SIGARCH Computer Architecture News, 1995 - ieexplore.ieee.org
... policies with varying **architectural** parameters. ... instruction prefetching, anti
speculative execution ... 2 358 2.1 **Branch** Prediction **Branch Target Buffers** (BTB) have ...
[Cited by 15](#) - [Web Search](#) - [BL Direct](#)

ProfileMe: Hardware Support for Instruction-Level Profiling on Out-of-Order Processors - group of 15 »

J Dean, JE Hicks, CA Waldspurger, WE Weihi, G ... - MICRO-ANNUAL WORKSHOP THEN ANNUAL
INTERNATIONAL SYMPOSIUM-, 1997 - waldspurger.org
... curs, the **speculative architectural** state is rolled back and fetching continues
after the most recent untrapped instruction (ie, the actual **branch target**). ...
[Cited by 122](#) - [View as HTML](#) - [Web Search](#) - [BL Direct](#)

Reducing **Branch** Costs via **Branch** Alignment - group of 9 »

B Calder, D Grunwald - ACM SIGOPS Operating Systems Review, 1994 - portal.acm.org
... algorithm that takes into consideration the **architectural** cost model ... **Branch** Prediction,
Profile-based Optimization, **Branch Target Buffers**, Trace Scheduling. ...
[Cited by 78](#) - [Web Search](#) - [BL Direct](#)

The Performance of Counter-and Correlation-Based Schemes for **Branch Target Buffers** - group of 8 »

A Mital - IEEE Transactions on Computers, 1995 - doi.ieeecs.org
... **Speculative** execution may also cause page ... Freudenberger, , "Predicting conditional
branch directions from ... **Architectural** Support for Programming Languages and ...
[Cited by 4](#) - [Web Search](#) - [BL Direct](#)

Dynamic **Branch** Prediction for a VLIW Processor - group of 7 »